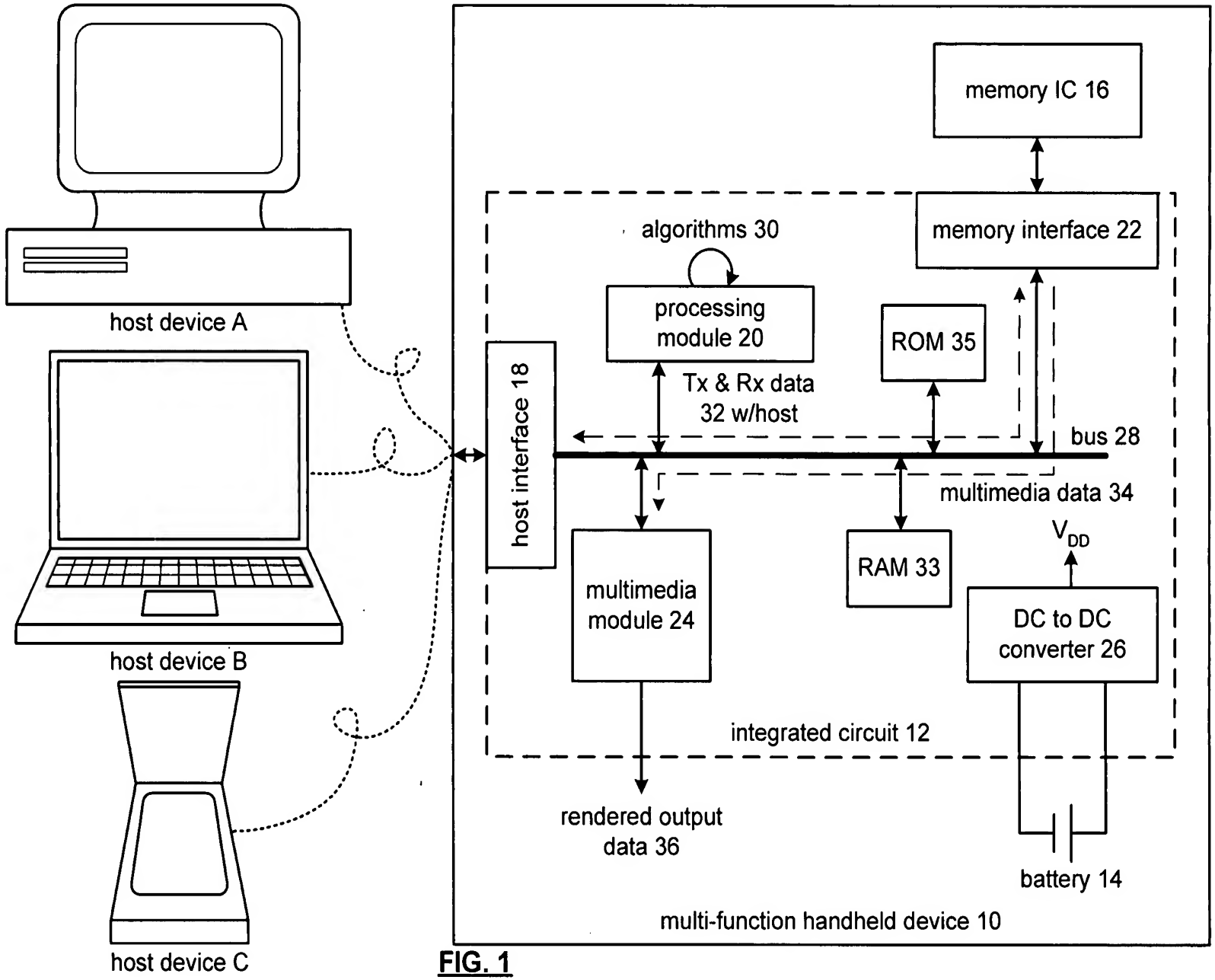

host device A
host device B
host device C
memory IC 16
memory interface 22
algorithms 30
processing module 20
ROM 35
Tx & Rx data 32 w/host
host interface 18
bus 28
multimedia data 34
multimedia module 24
RAM 33
V_{DD}
DC to DC converter 26
integrated circuit 12
rendered output data 36
battery 14
multi-function handheld device 10

FIG. 1

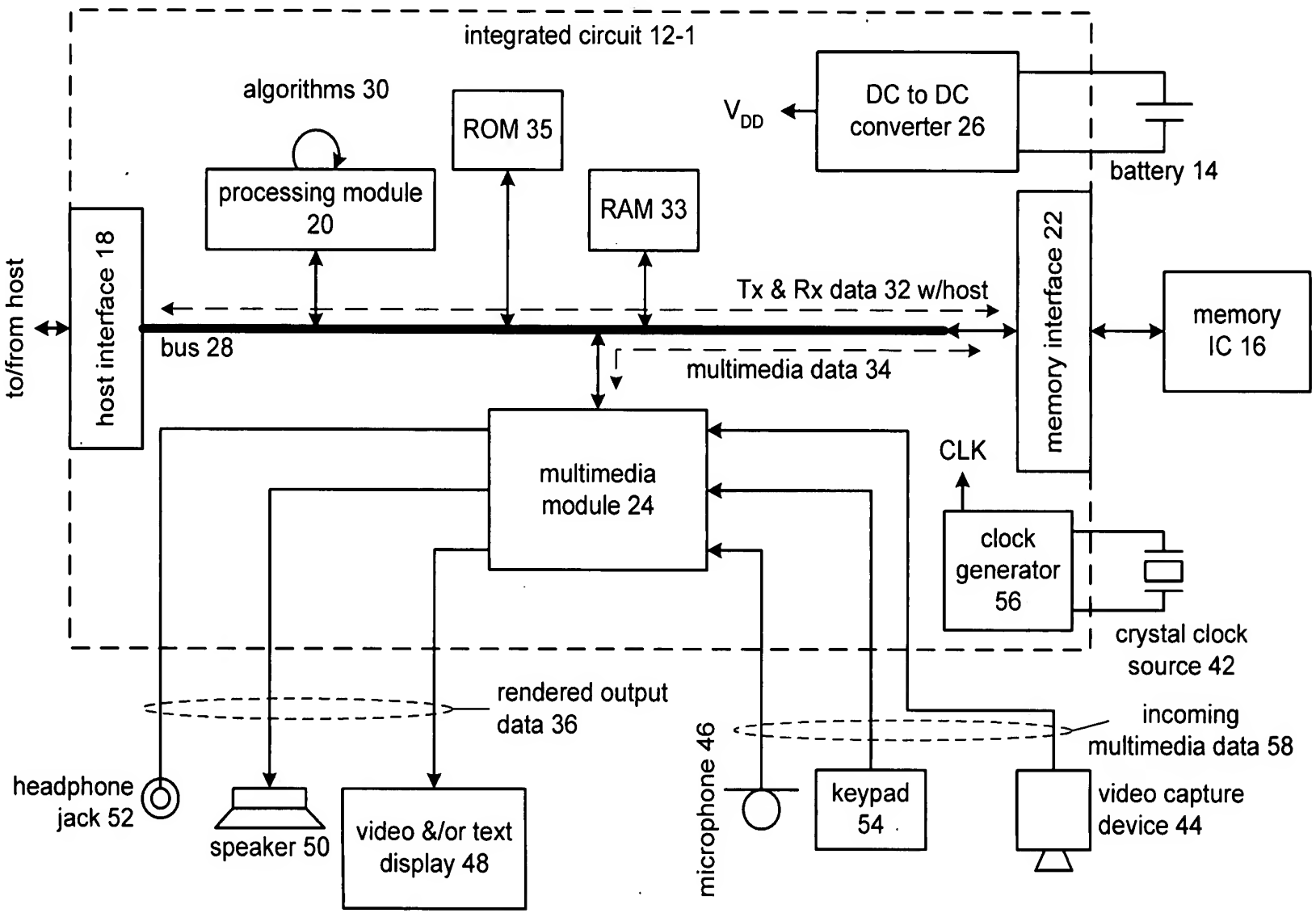


FIG. 2

multi-function handheld device 40

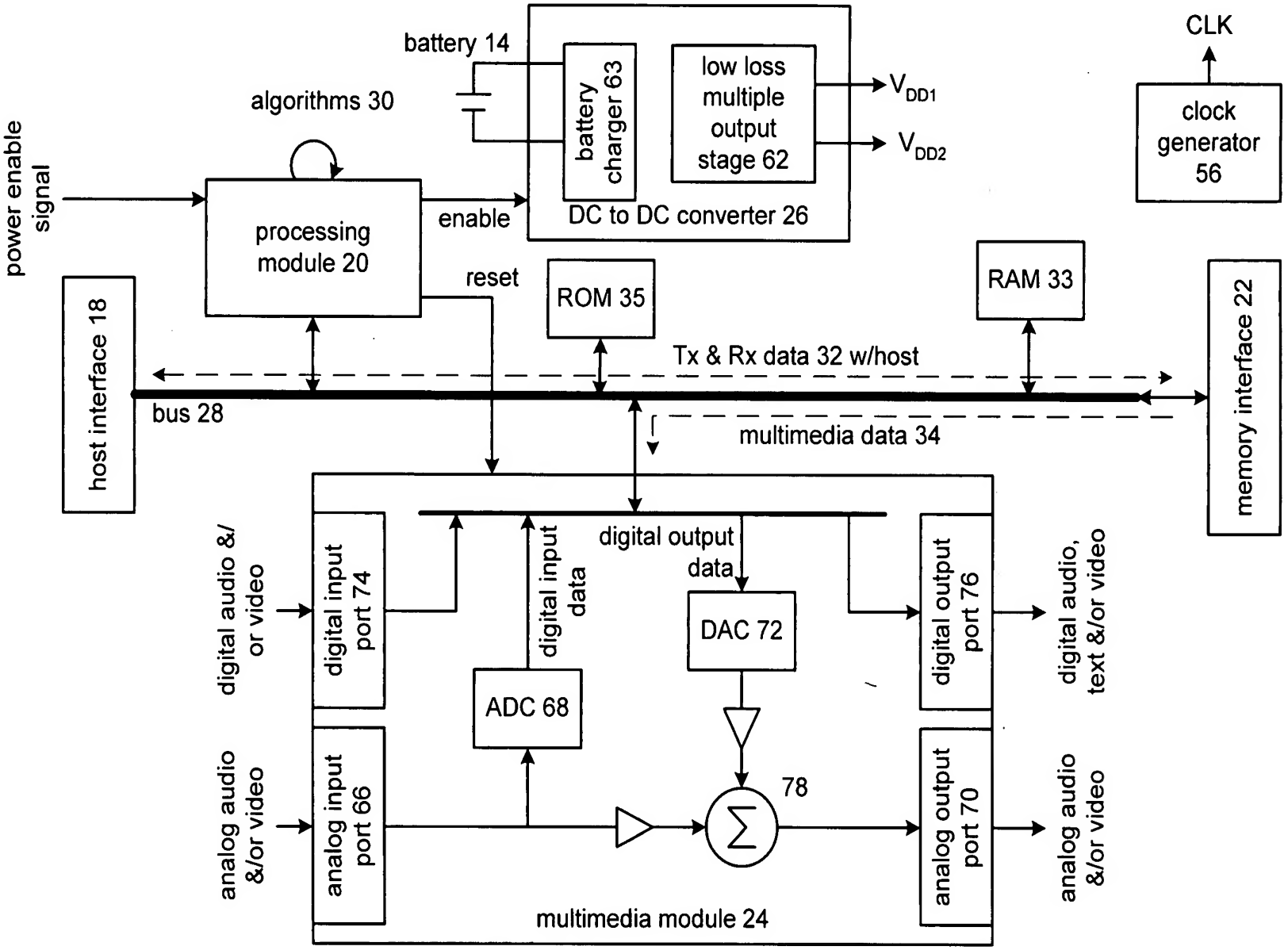


FIG. 3

integrated circuit 12-2

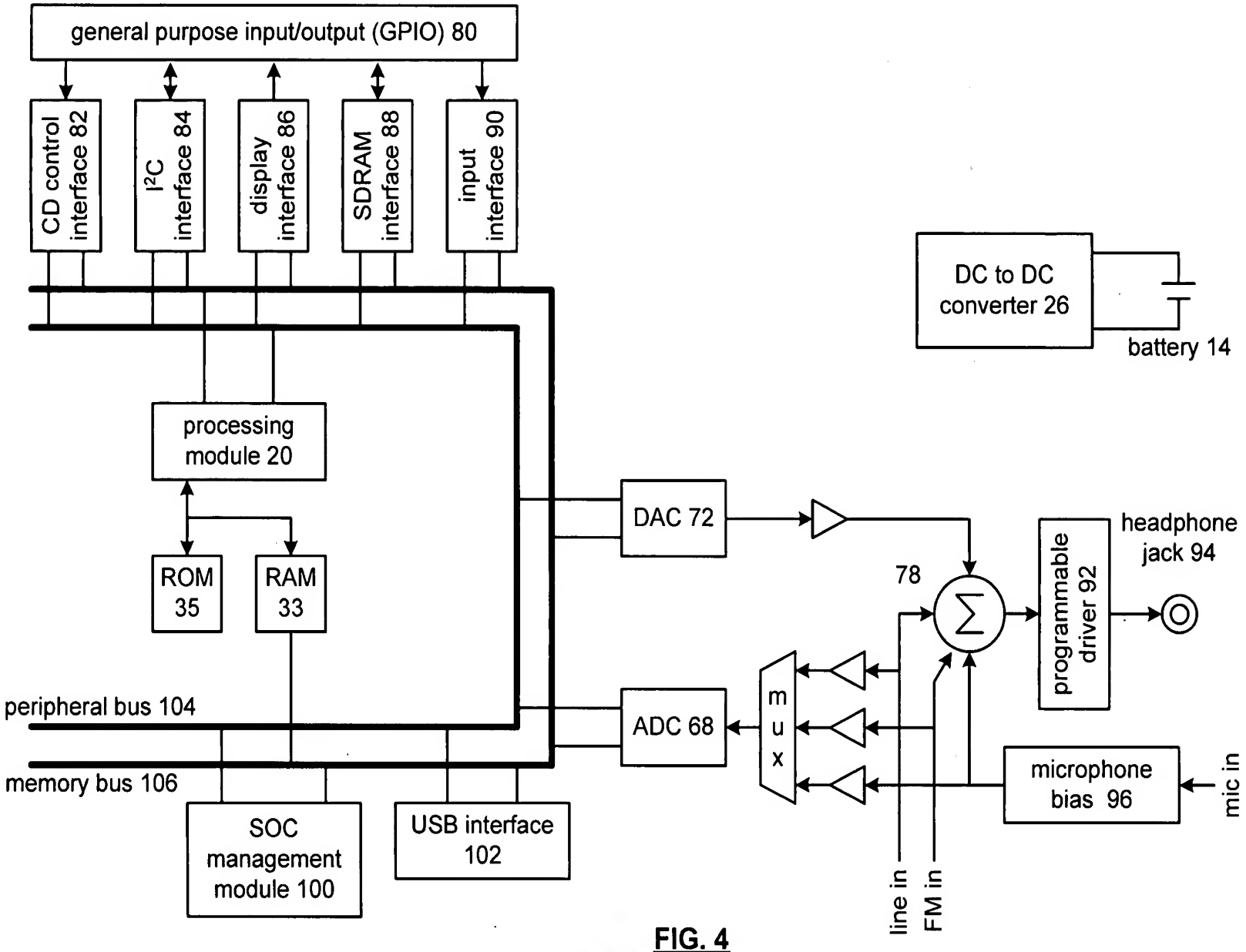


FIG. 4

integrated circuit 12-3

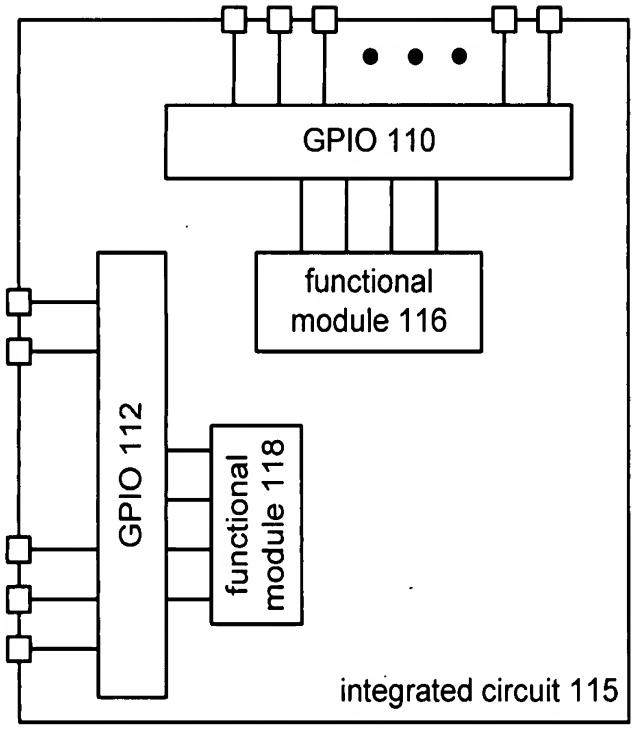


FIG. 5

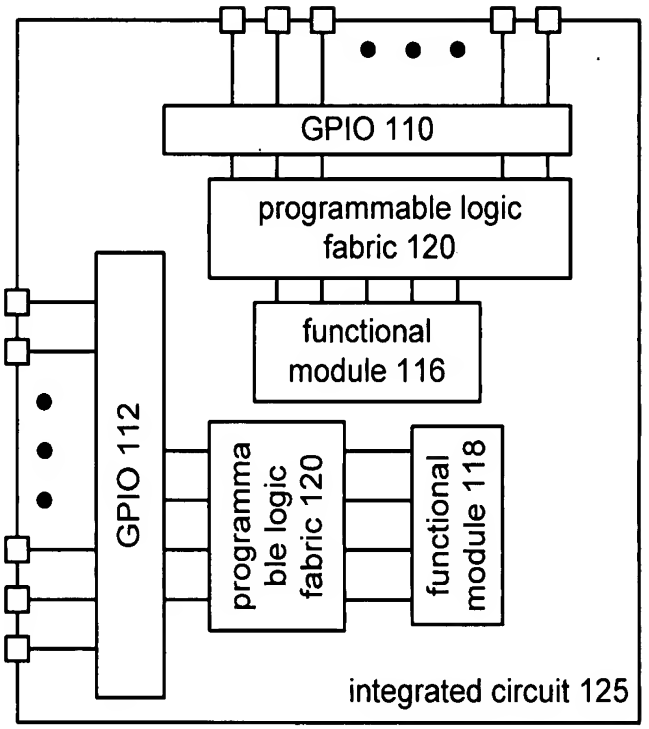


FIG. 6

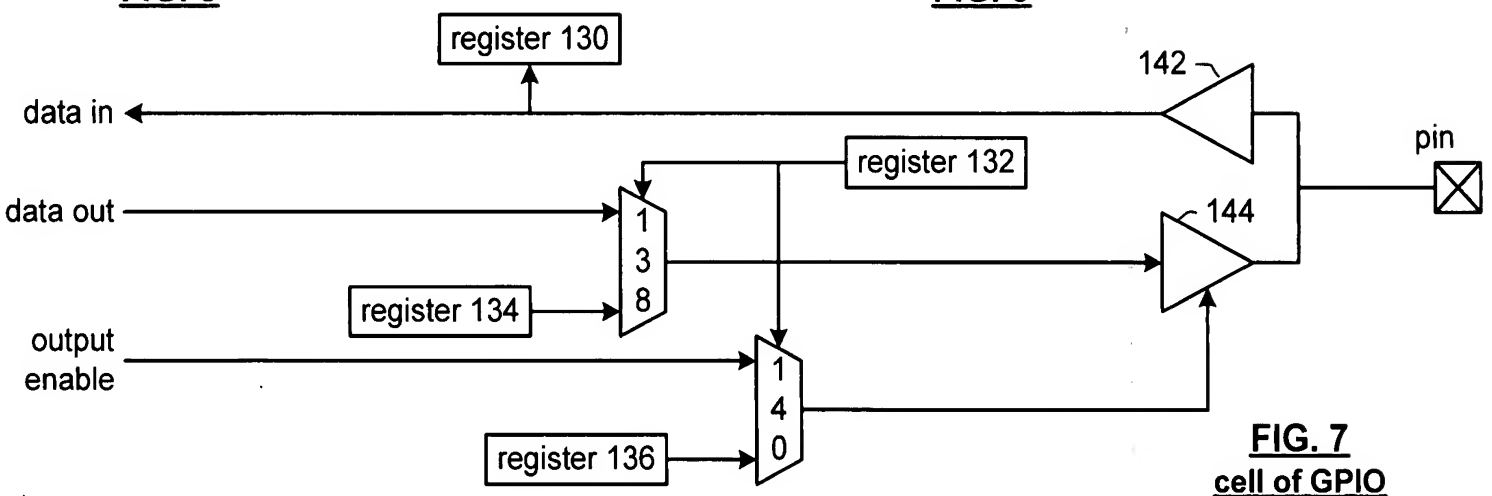


FIG. 7
cell of GPIO

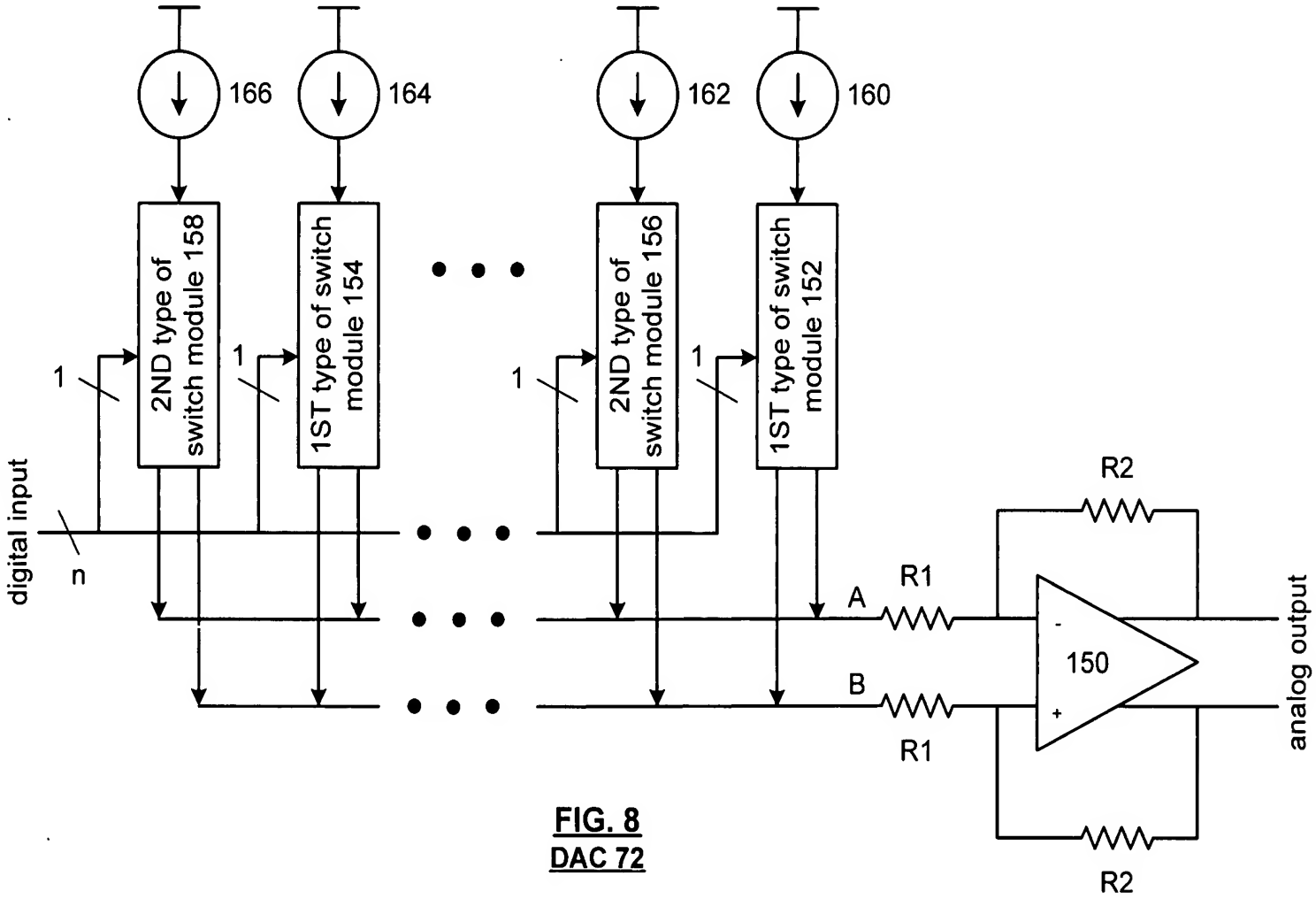

166
164
162
160
2ND type of switch module 158
1ST type of switch module 154
2ND type of switch module 156
1ST type of switch module 152
1
1
1
1
digital input
n
R2
R1
A
B
R1
150
analog output
R2

FIG. 8
DAC 72

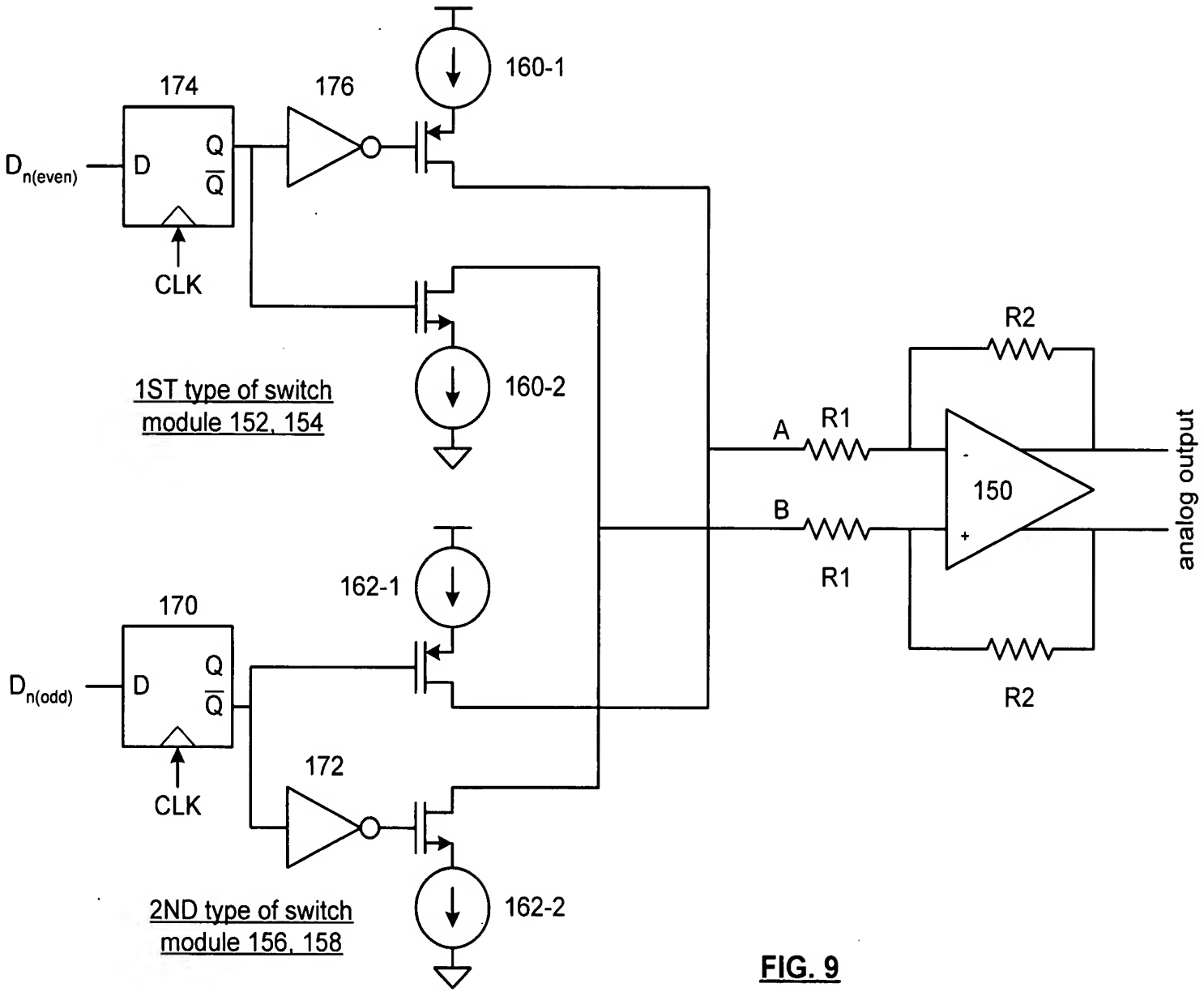

174
176
160-1
D
Q
$\overline{Q}$
$D_{n(even)}$
CLK
160-2
1ST type of switch
module 152, 154
R2
A
R1
B
R1
150
analog output
R2
162-1
170
$D_{n(odd)}$
172
CLK
162-2
2ND type of switch
module 156, 158

FIG. 9

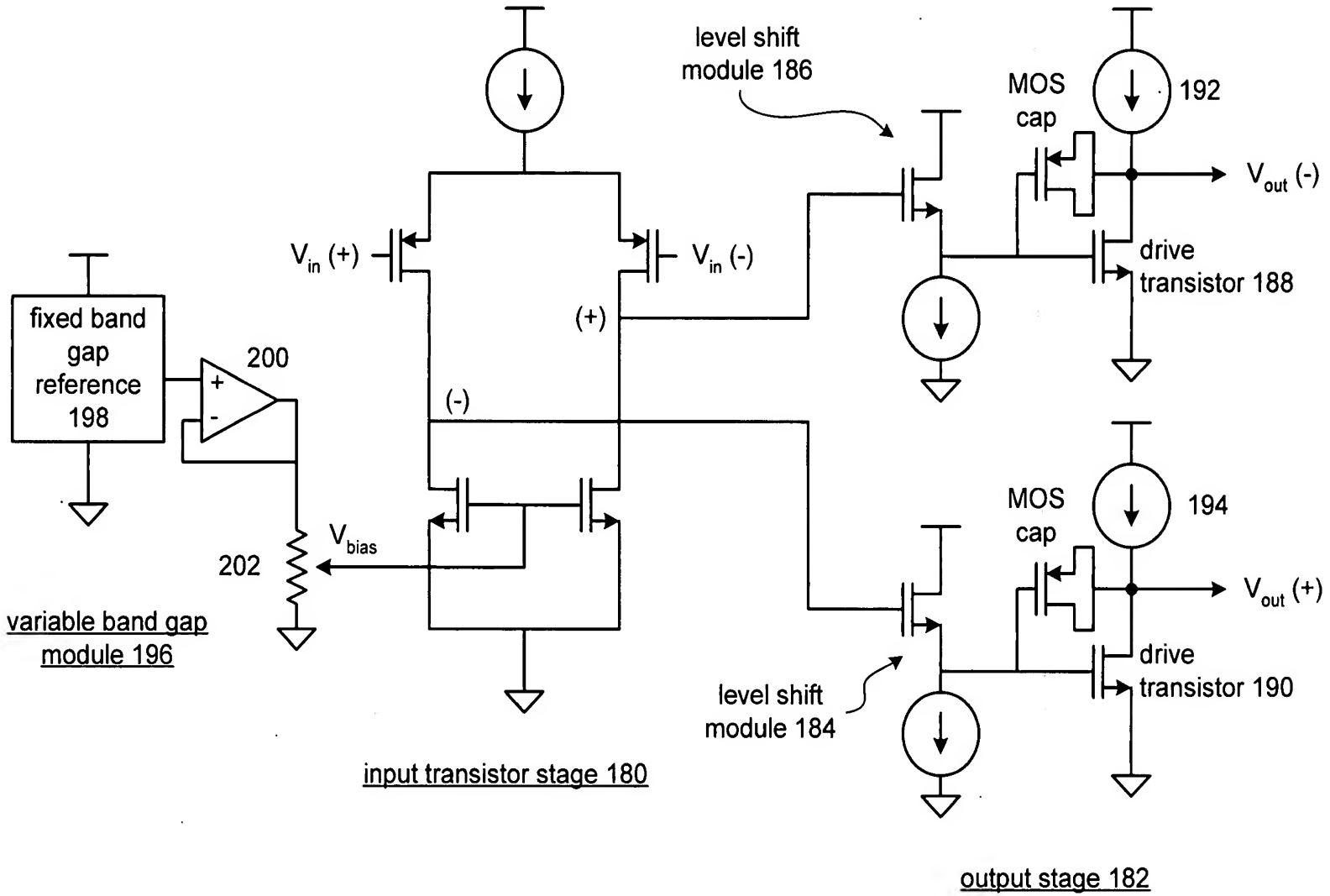


FIG. 10
op amp 150

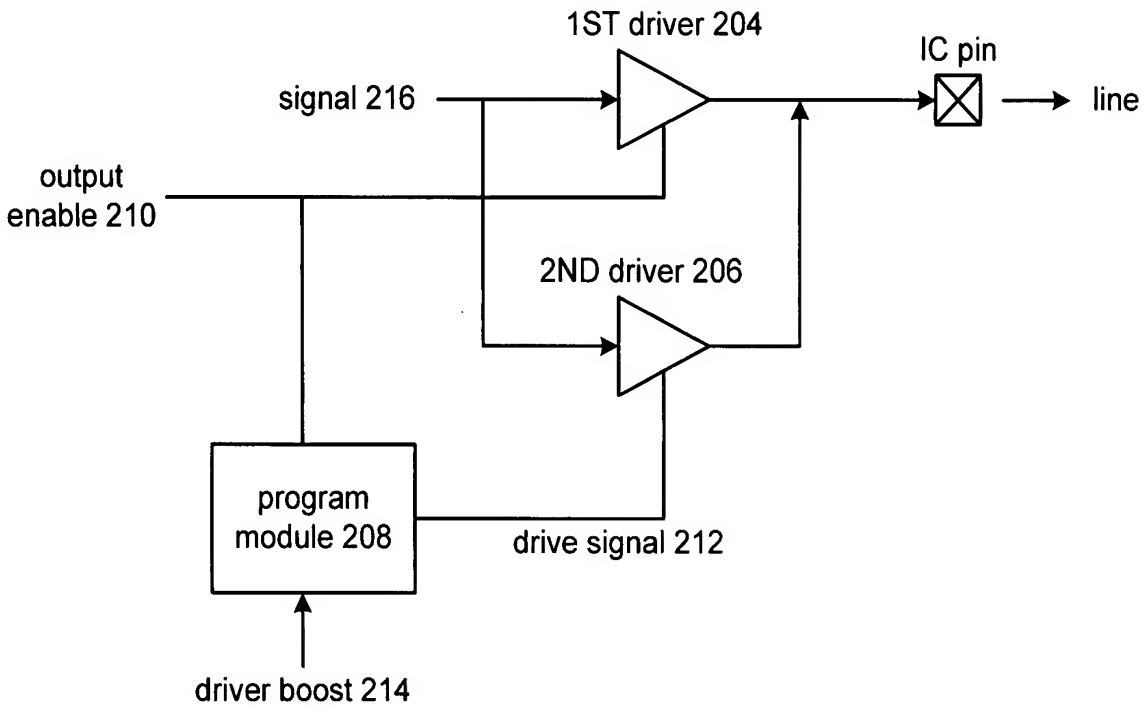


FIG. 11
programmable driver 92

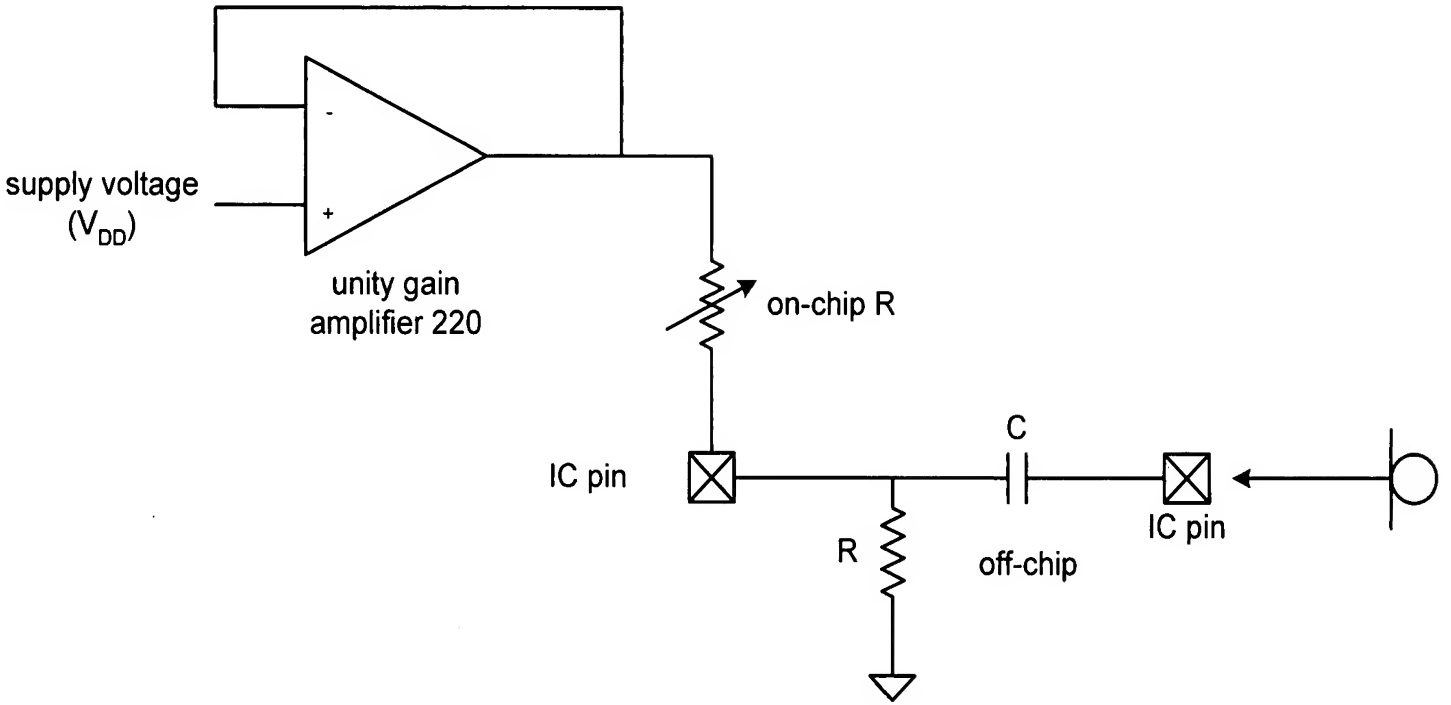


FIG. 12
microphone bias 96

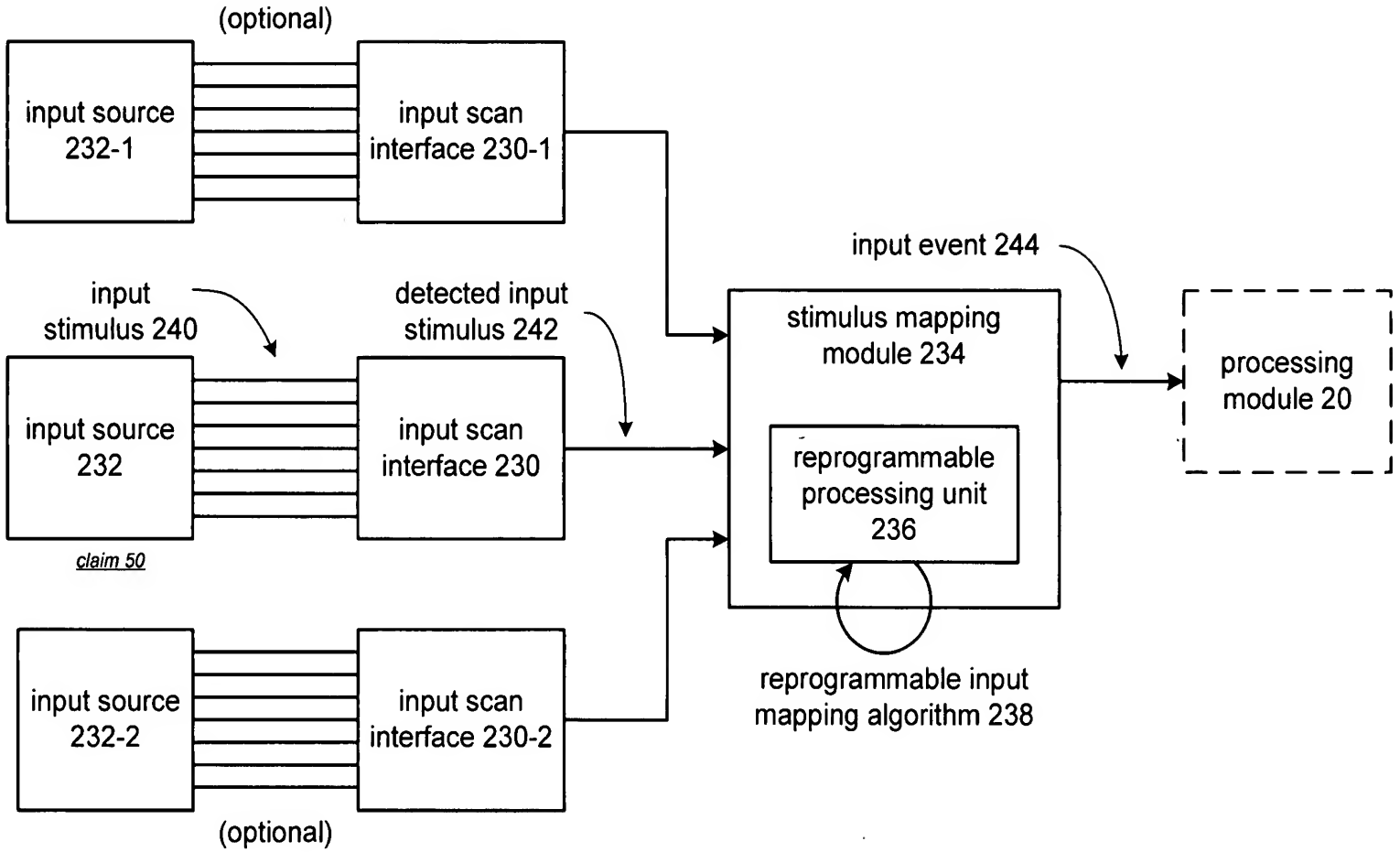


FIG. 13
input interface 90

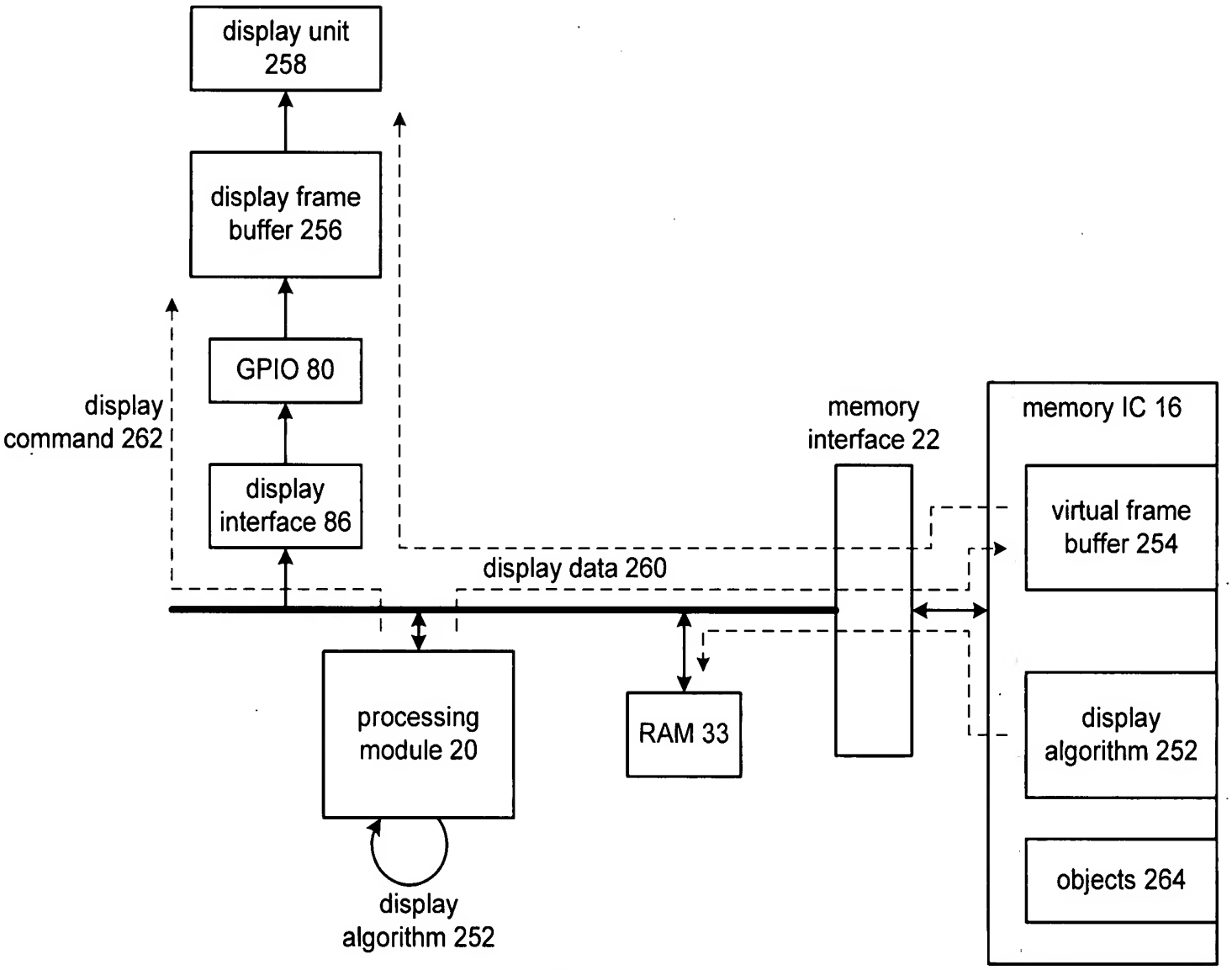


FIG. 14

display interface system 250

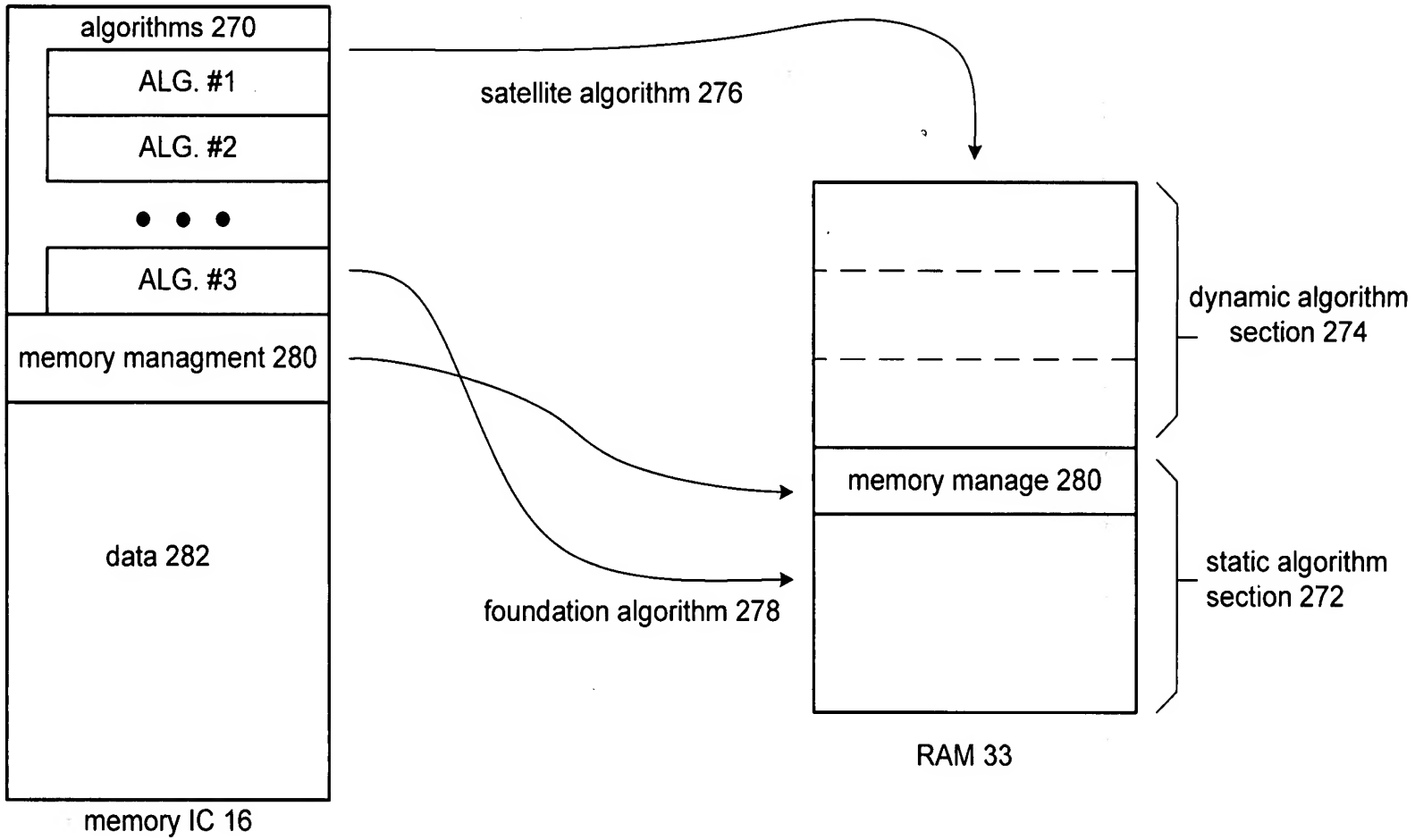

algorithms 270
ALG. #1
ALG. #2
ALG. #3
memory managment 280
data 282
memory IC 16
satellite algorithm 276
foundation algorithm 278
memory manage 280
dynamic algorithm section 274
static algorithm section 272
RAM 33

FIG. 15

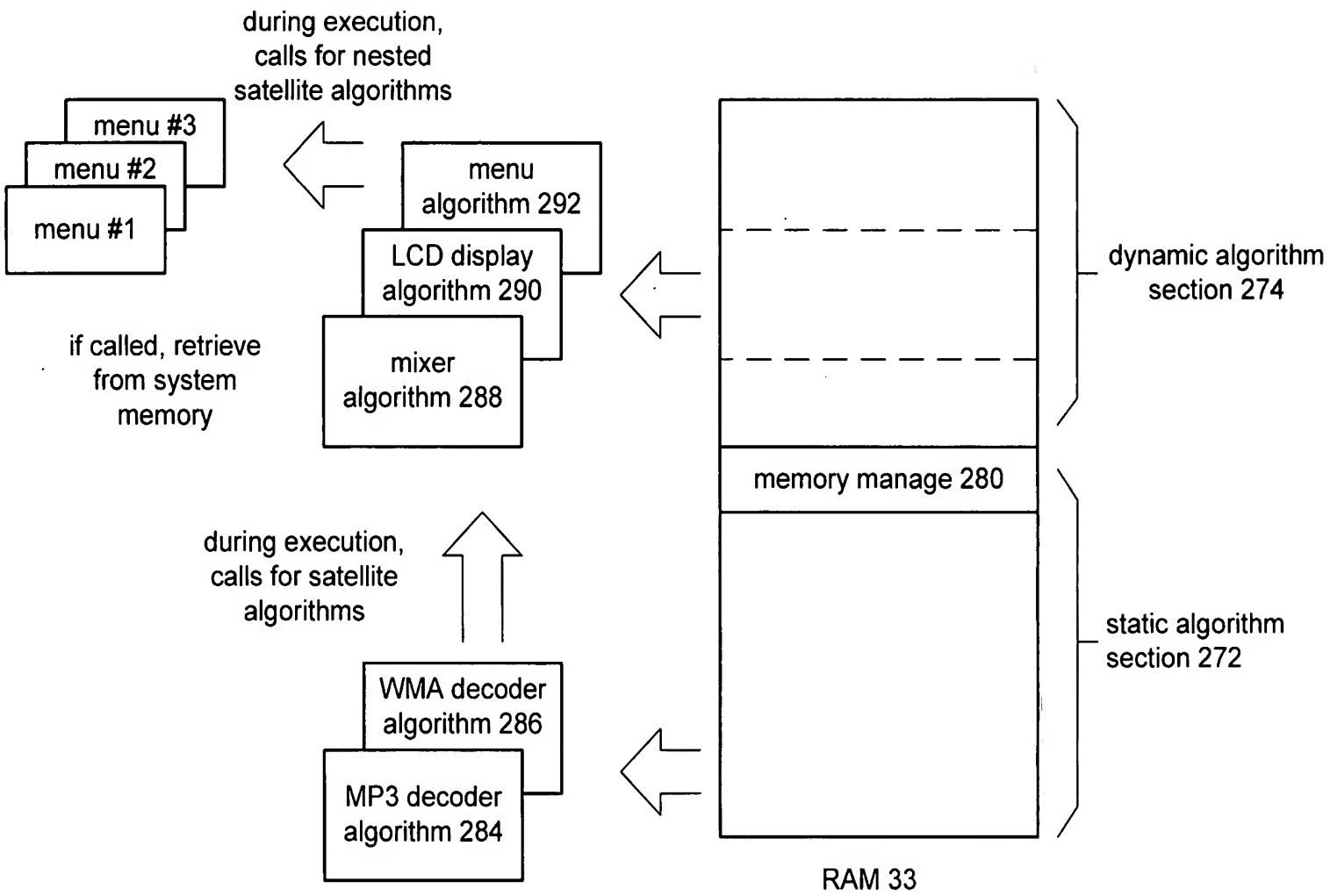

during execution,
calls for nested
satellite algorithms
menu #3
menu #2
menu #1
menu
algorithm 292
LCD display
algorithm 290
mixer
algorithm 288
if called, retrieve
from system
memory
dynamic algorithm
section 274
memory manage 280
during execution,
calls for satellite
algorithms
WMA decoder
algorithm 286
MP3 decoder
algorithm 284
static algorithm
section 272
RAM 33

FIG. 16

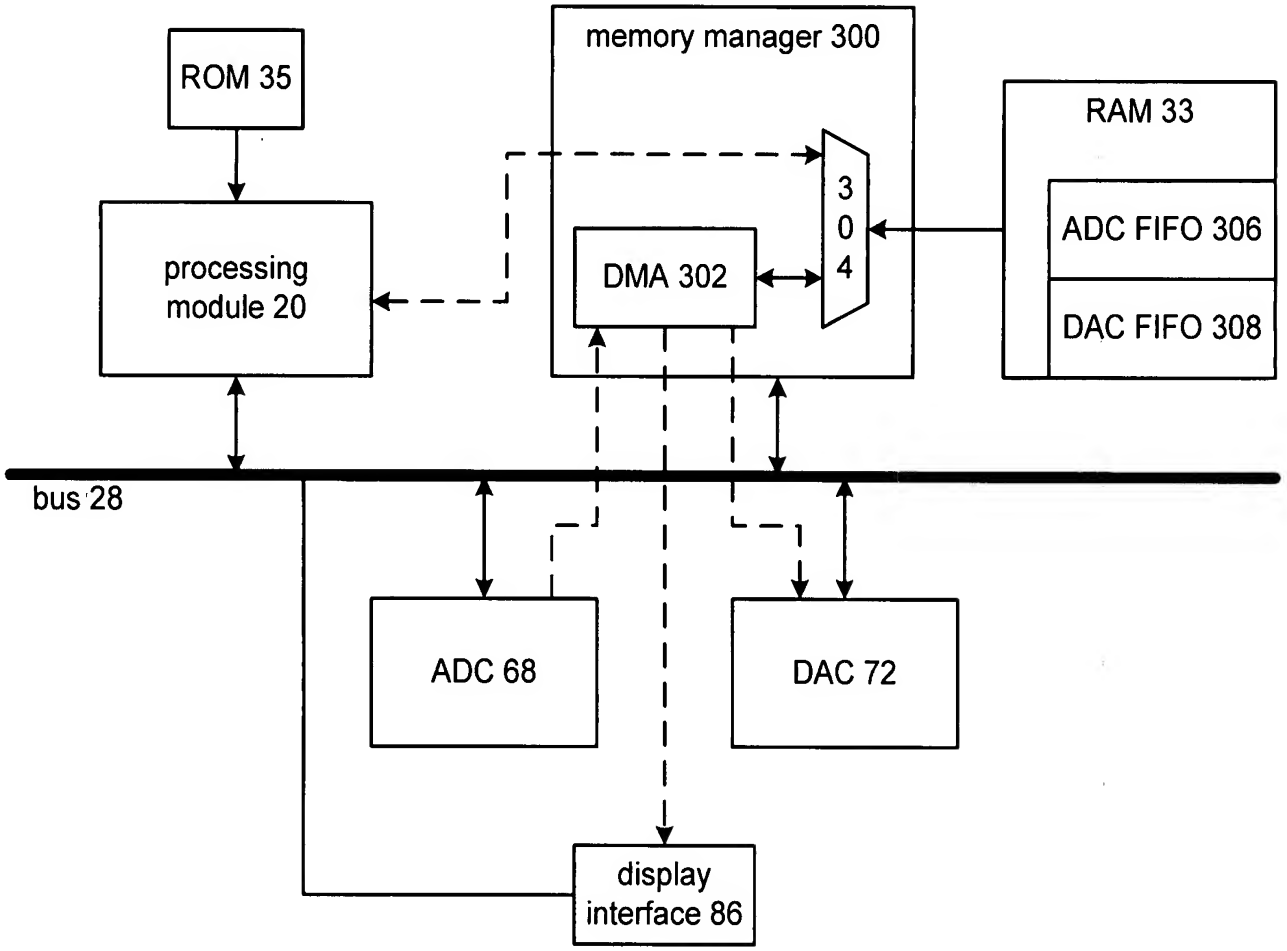
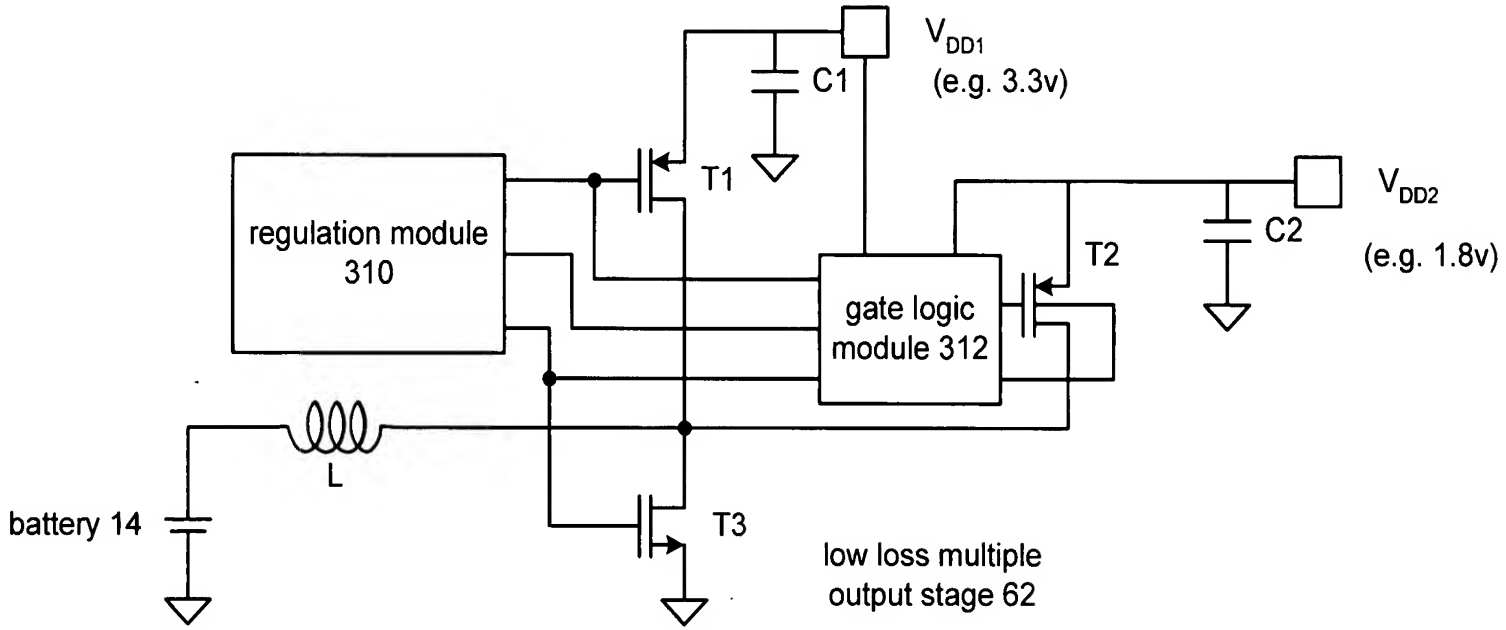

memory manager 300
ROM 35
RAM 33
3
0
4
ADC FIFO 306
processing
module 20
DMA 302
DAC FIFO 308
bus 28
ADC 68
DAC 72
display
interface 86

FIG. 17



gate logic module function

if T1 is on, set gate and well voltage of T2 to V_{DD1};
if T1 is off and T3 is on, set gate and well voltage of T2 to V_{DD2};
if T1 is off and T2 is on, set gate and well voltage of T2 to 0v

FIG. 18
DC to DC converter 26

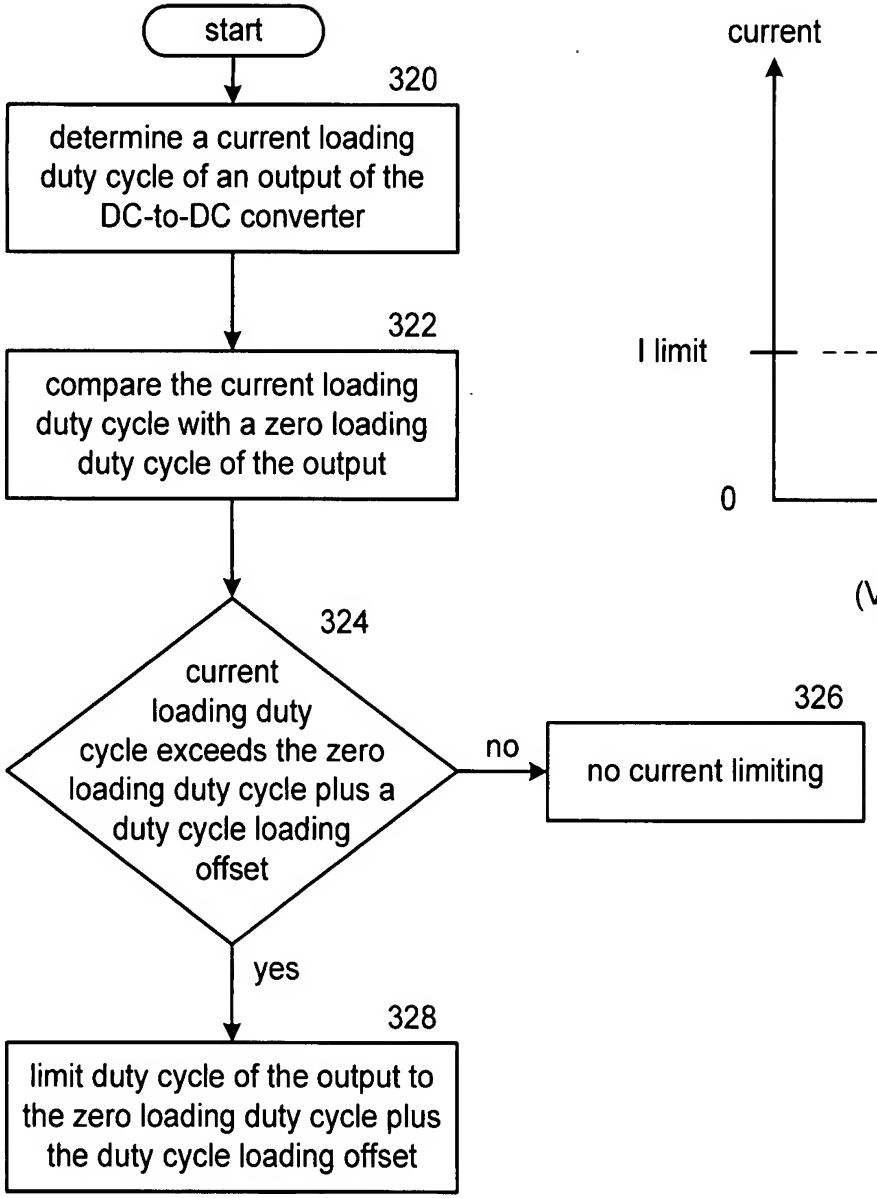

start
320
determine a current loading duty cycle of an output of the DC-to-DC converter
322
compare the current loading duty cycle with a zero loading duty cycle of the output
324
current loading duty cycle exceeds the zero loading duty cycle plus a duty cycle loading offset
no
326
no current limiting
yes
328
limit duty cycle of the output to the zero loading duty cycle plus the duty cycle loading offset

FIG. 19

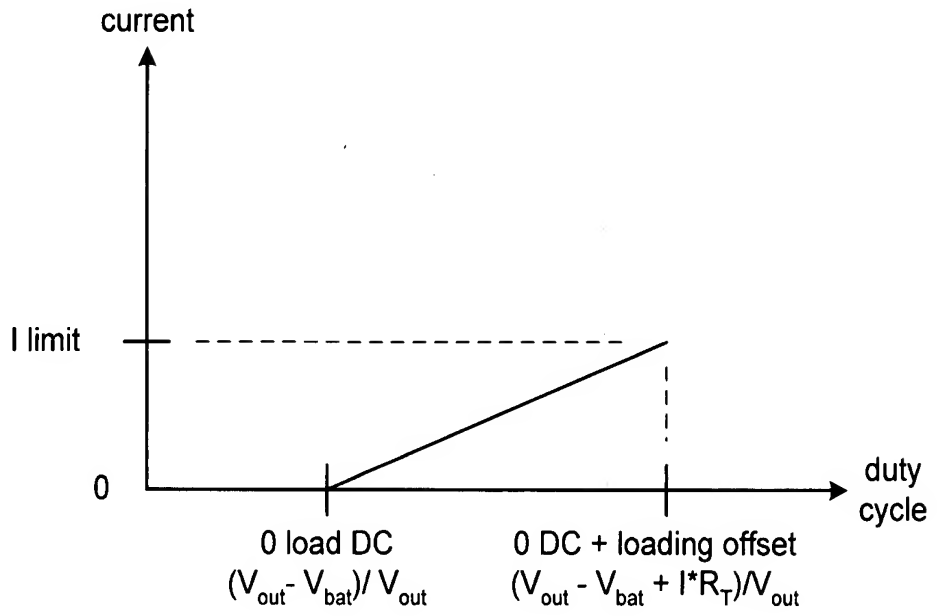

current
I limit
0
duty cycle
0 load DC
$(V_{out} - V_{bat})/ V_{out}$
0 DC + loading offset
$(V_{out} - V_{bat} + I*R_T)/V_{out}$

FIG. 20

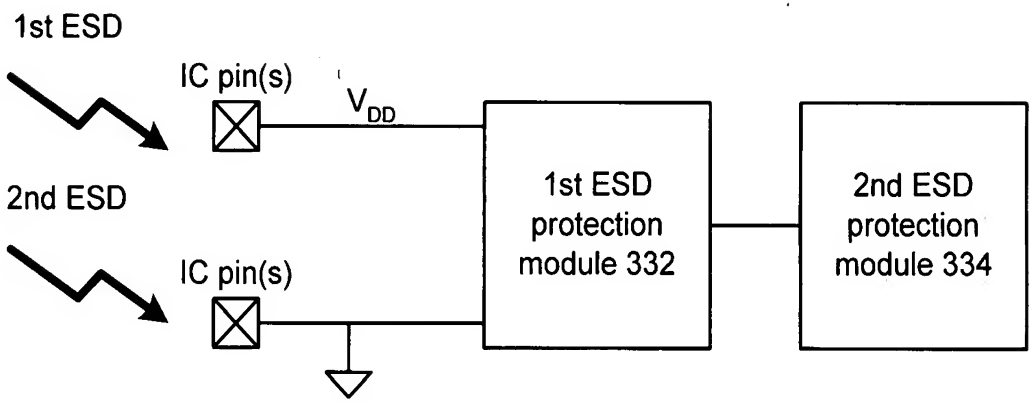


FIG. 21
ESD protection circuit 330

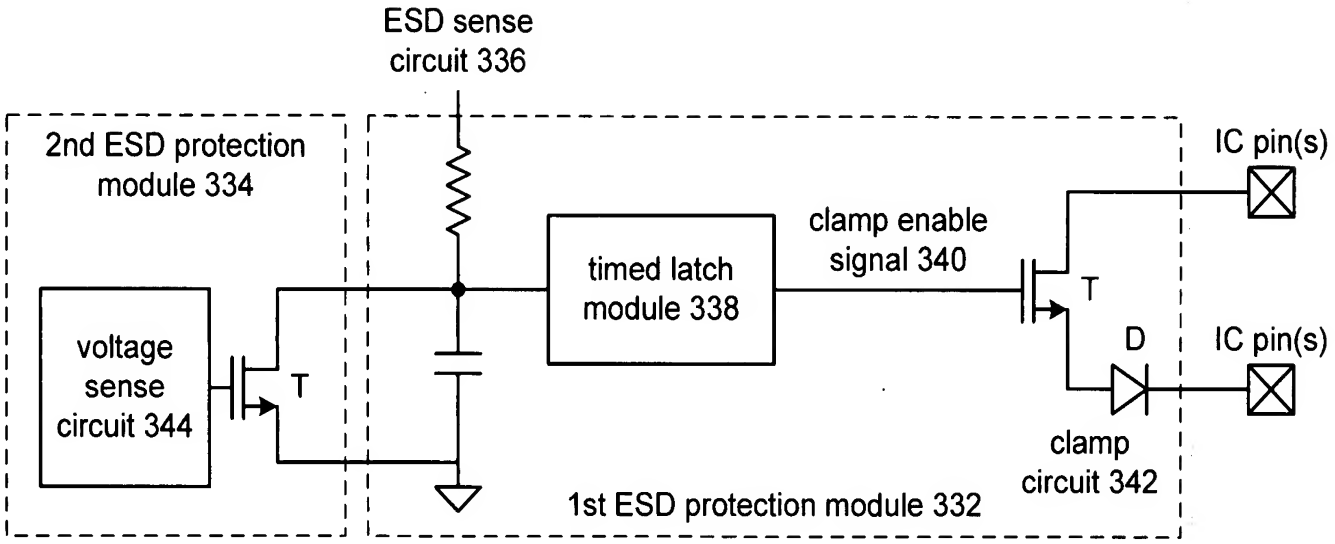


FIG. 22
ESD protection circuit 335

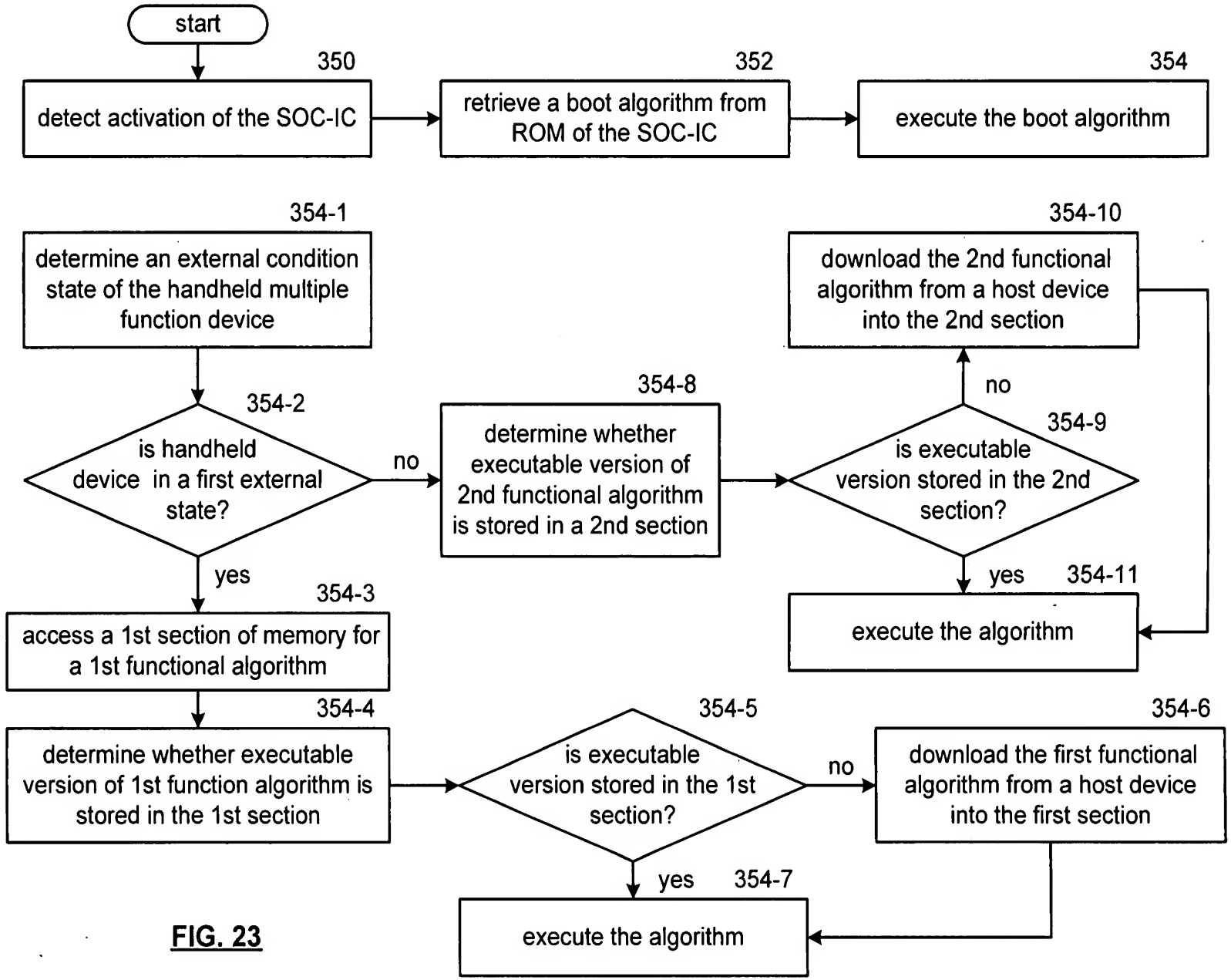

start
350
detect activation of the SOC-IC
352
retrieve a boot algorithm from ROM of the SOC-IC
354
execute the boot algorithm
354-1
determine an external condition state of the handheld multiple function device
354-2
is handheld device in a first external state?
no
yes
354-3
access a 1st section of memory for a 1st functional algorithm
354-4
determine whether executable version of 1st function algorithm is stored in the 1st section
354-5
is executable version stored in the 1st section?
no
yes
354-6
download the first functional algorithm from a host device into the first section
354-7
execute the algorithm
354-8
determine whether executable version of 2nd functional algorithm is stored in a 2nd section
354-9
is executable version stored in the 2nd section?
no
yes
354-10
download the 2nd functional algorithm from a host device into the 2nd section
354-11
execute the algorithm

FIG. 23

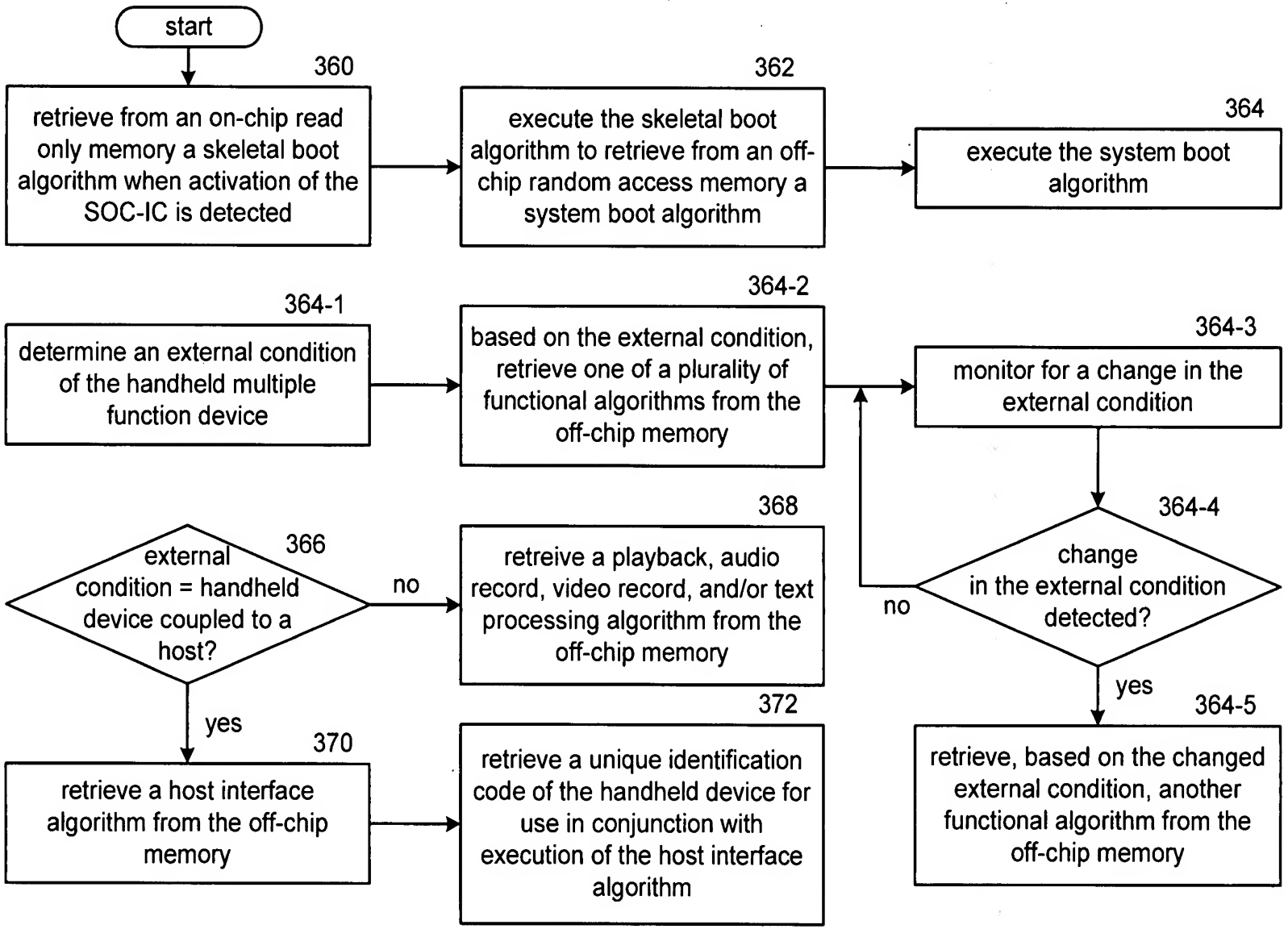

start
360
retrieve from an on-chip read only memory a skeletal boot algorithm when activation of the SOC-IC is detected
362
execute the skeletal boot algorithm to retrieve from an off-chip random access memory a system boot algorithm
364
execute the system boot algorithm
364-1
determine an external condition of the handheld multiple function device
364-2
based on the external condition, retrieve one of a plurality of functional algorithms from the off-chip memory
364-3
monitor for a change in the external condition
364-4
change in the external condition detected?
no
yes
366
external condition = handheld device coupled to a host?
no
yes
368
retreive a playback, audio record, video record, and/or text processing algorithm from the off-chip memory
370
retrieve a host interface algorithm from the off-chip memory
372
retrieve a unique identification code of the handheld device for use in conjunction with execution of the host interface algorithm
364-5
retrieve, based on the changed external condition, another functional algorithm from the off-chip memory

FIG. 24

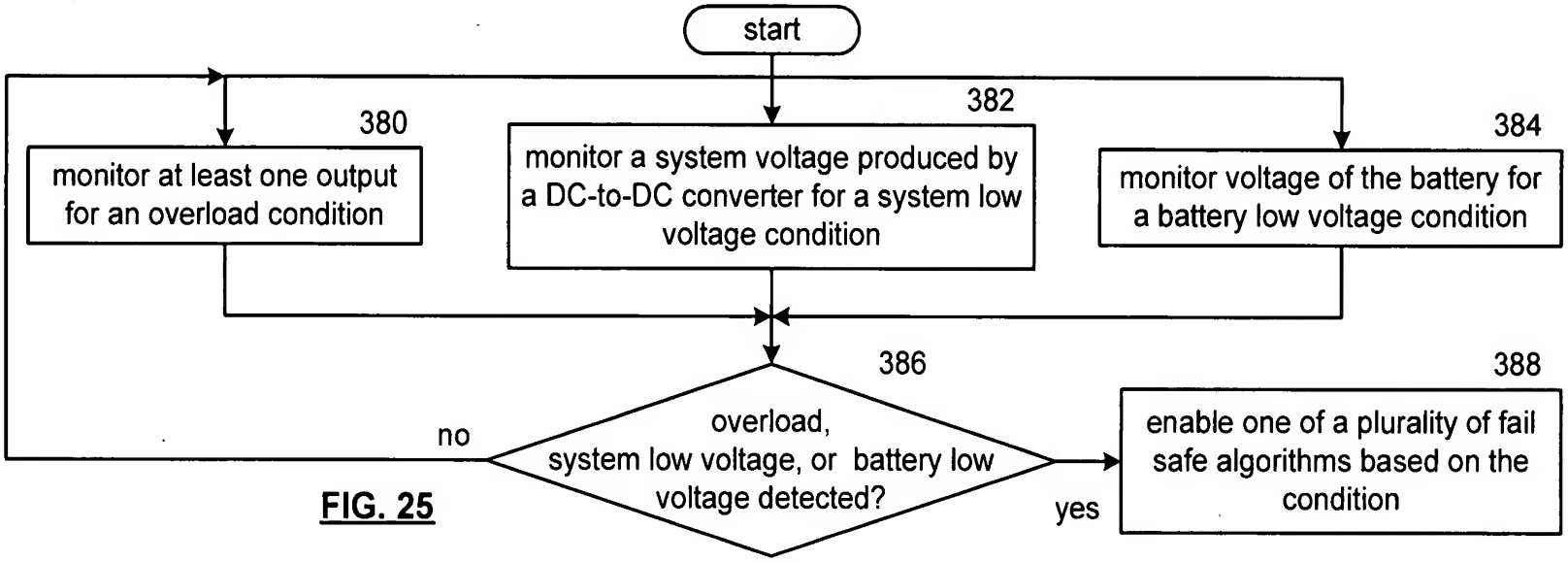


FIG. 25

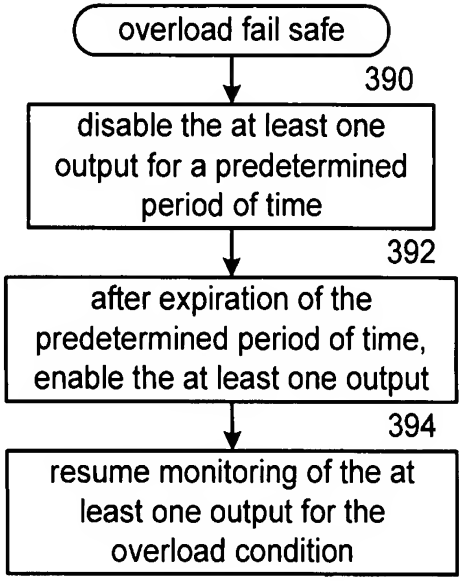


FIG. 26

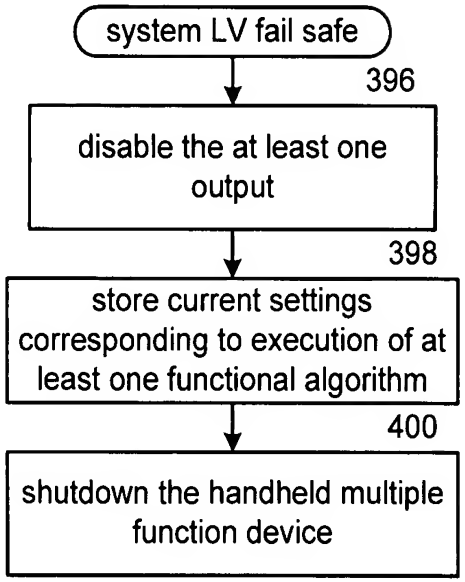


FIG. 27

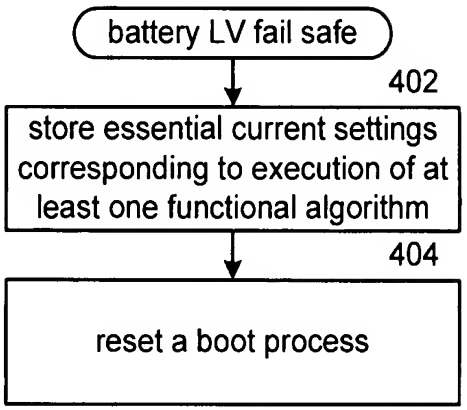


FIG. 28

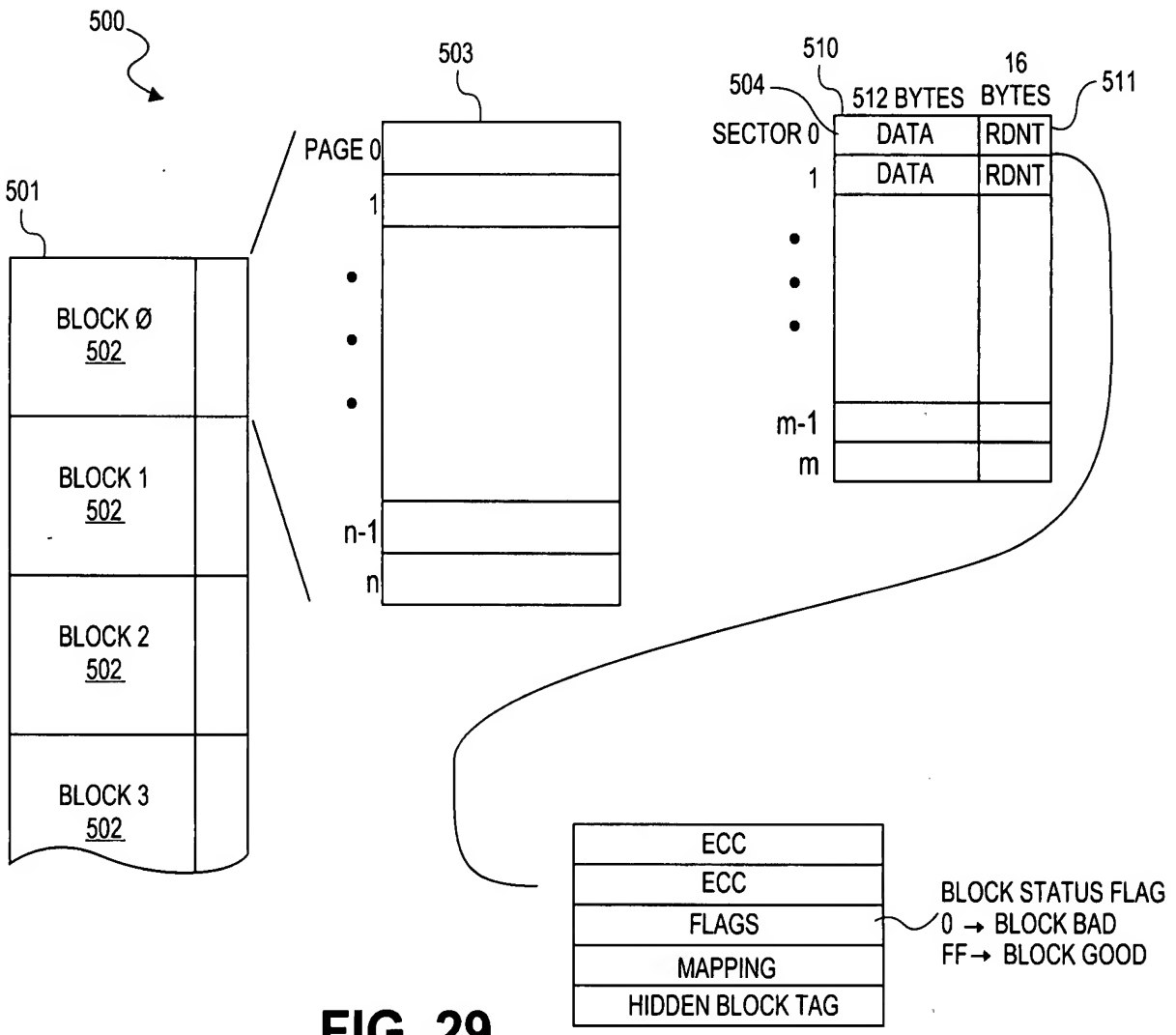

500
501
BLOCK Ø
502
BLOCK 1
502
BLOCK 2
502
BLOCK 3
502
503
PAGE 0
1
n-1
n
510
504
512 BYTES
16
BYTES
511
SECTOR 0
DATA
RDNT
1
DATA
RDNT
m-1
m
ECC
ECC
FLAGS
MAPPING
HIDDEN BLOCK TAG
BLOCK STATUS FLAG
0 → BLOCK BAD
FF → BLOCK GOOD

FIG. 29

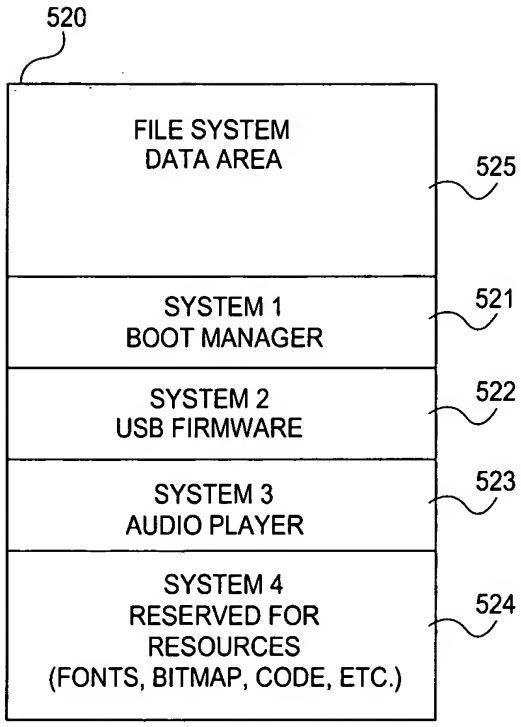

520
FILE SYSTEM
DATA AREA
525
SYSTEM 1
BOOT MANAGER
521
SYSTEM 2
USB FIRMWARE
522
SYSTEM 3
AUDIO PLAYER
523
SYSTEM 4
RESERVED FOR
RESOURCES
(FONTS, BITMAP, CODE, ETC.)
524

FIG. 30

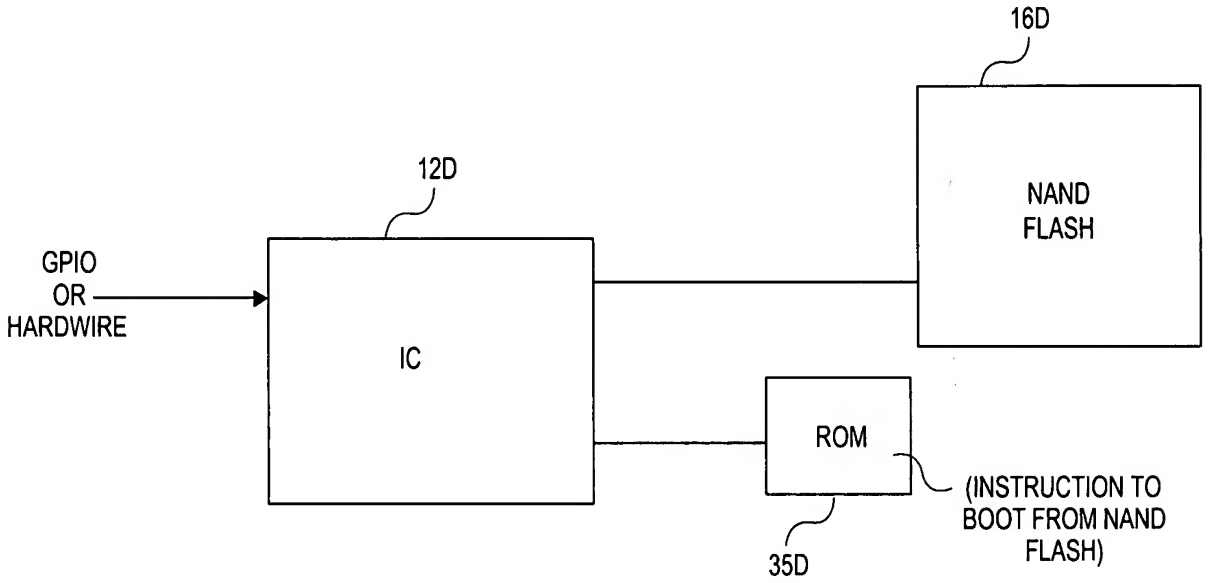

16D
NAND
FLASH
12D
GPIO
OR
HARDWIRE
IC
ROM
(INSTRUCTION TO
BOOT FROM NAND
FLASH)
35D

FIG. 31

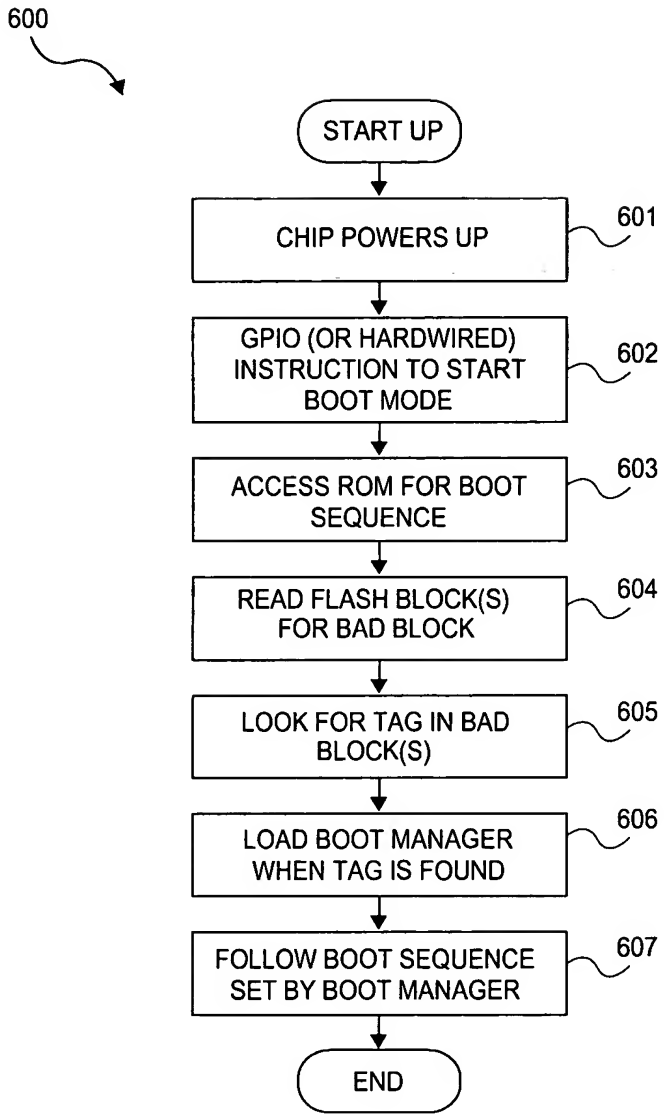

600
START UP
CHIP POWERS UP
601
GPIO (OR HARDWIRED) INSTRUCTION TO START BOOT MODE
602
ACCESS ROM FOR BOOT SEQUENCE
603
READ FLASH BLOCK(S) FOR BAD BLOCK
604
LOOK FOR TAG IN BAD BLOCK(S)
605
LOAD BOOT MANAGER WHEN TAG IS FOUND
606
FOLLOW BOOT SEQUENCE SET BY BOOT MANAGER
607
END

FIG. 32